Notice of Allowability Ex	Application No.	Applicant(s)
	09/650,329	ADAMS ET AL.
	Examiner	Art Unit
	Ngoc K. Vu	2611
The MAILING DATE of this communication appears on the cover sheet with the correspondence address All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.		
1. This communication is responsive to <u>1/12/06</u> .		
2. The allowed claim(s) is/are <u>4,8,9,13 and 17-26</u> .		
3.		
Attachment(s) 1. ☑ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) 3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/06 Paper No./Mail Date 4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	6. ☐ Interview Summary Paper No./Mail Da 8), 7. ☑ Examiner's Amend	te

EXAMINER'S AMENDMENT

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An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR
 To ensure consideration of such an amendment, it MUST be submitted no later than the

Authorization for this examiner's amendment was given in a telephone interview with

The application has been amended as follows:

In the claim:

payment of the issue fee.

Michael Drapkin on March 08, 2006.

Claim 4, lines 15-16, "a system timestamp from an application system coupled with the decoder circuit but not with the receiver circuit" has been changed into --a second STC timestamp--.

Claim 4, line 17, "the system timestamp" has been changed into --a system timestamp--.

Claim 4, line 18, "the decoder circuit" has been changed into --the second STC timestamp--, "the first STC timestamp captured by the receiver circuit to" has been changed into --a last PCR timestamp received--.

Claim 7 is canceled.

Claim 8, lines 1-2, "the application system comprises an audio-visual system and" has been deleted.

Claim 9, lines 1-2, "the application system comprises a networked computer system and" has been deleted.

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Claim 13, line 13, "the STC timestamp" has been changed into --the first STC timestamp--.

Claim 13, line 16, "result;" has been changed into --result by using firmware within the receiver circuit;--.

Claim 13, lines 17-19, "a second latch in the decoder circuit, the second latch being adapted to capture a system timestamp from an application system coupled with the decoder circuit but not with the receiver circuit" has been changed into --the decoder circuit configured to capture a second STC timestamp--.

Claim 13, lines 20-21, "(d) a second adjuster coupled to the decoder circuit, the second adjuster being adapted to adjust the" has been changed into --wherein the system adjusts a--.

Claim 13, lines 22-23, "the decoder circuit and the first STC timestamp captured by the receiver circuit to maintain synchronization between the decoder circuit and the receiver circuit" has been changed into --the second STC timestamp and a last PCR timestamp received--.

Claim 16 is canceled.

Claim 17, lines 1-2, "the application system comprises an audio-visual system and" has been deleted.

Claim 18, lines 1-2, "the application system comprises a networked computer system and" has been deleted.

Claim **20**, line 14, "result using the receiver circuit;" has been changed into --result by using firmware within the receiver circuit;--.

Claim 20, line 15, "receiving data from the decoder circuit" has been changed into -- writing--.

Claim 20, line 16, "comprised by the bus" has been deleted.

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Claim 20, line 18, "after receiving the data from the decoder circuit; and " has been changed into --, wherein the writing into the first register causes the second STC timestamp to be latched into the second register; and--.

Claim **20**, line 19, "providing the second STC timestamp" has been changed into -- retrieving the second STC timestamp--.

Claim 24, line 14, "the STC timestamp" has been changed into --the first STC timestamp--.

Claim 24, line 17, "result;" has been changed into --result by using firmware within the receiver circuit;--.

Claim **24**, lines 18-19, "comprised by the host-system bus, the first register being adapted to receive data from the decoder circuit" has been deleted.

Claim 24, line 21, "after the first register receives the data from the decoder circuit," has been changed into --, wherein writing into the first register causes the second STC timestamp to be latched into the second register--.

- 2. Claims 4, 8, 9, 13 and 17-26 are allowed.
- 3. The following is an examiner's statement of reasons for allowance:

The closest prior arts, Inazumi et al. (US 6,731,658 B1) teach a data recording method and a data recording apparatus. Particularly, apparatus 100 comprises a decoder 28, a receiving section 11 coupled to a bus 29 via multiplexer 12 and CPU 13 coupled to the bus 29. The CPU is configured to conduct operations of the apparatus 100. (See figure 3). Inazumi further discloses that PCR is used to synchronize program data and apparatus 100 shown in figure 3, i.e., a transmitter (not shown) for transmitting TS data 1 and the apparatus 100, in recording or reproducing the program data within the TS data 1 by the apparatus 100. The apparatus 100 compares the value of the PCR with the value of the internal clock and calculates

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the difference of the both every when it receives the PCR disposed in the TS data 1 transmitted from the transmitter. Then, the apparatus 100 sets or calibrates the frequency of the reference clock signal as to eliminate this difference. Thereby, it becomes possible to synchronize the transmitter transmitting the TS data and the apparatus 100 and to reproduce or record the program data multiplexed into the TS data 1 transmitted from the transmitter at high precision. (See col. 6, line 4 to col. 7, line 51).

Inazumi et al fail to teach or fairly suggest the feature of "coupling the receiver circuit with the decoder circuit and the microprocessor, wherein the receiver circuit, decoder circuit, microprocessor each comprise separate nodes of a bus in the host computer", "capturing, with the decoder circuit, a second STC timestamp; and adjusting a system timestamp with an offset on a message delay time between the second STC timestamp and a last PRC timestamp received" as recited in claim 4 and similarly recited in claim 13; "a bus in the host computer having the microprocessor, the receiver circuit and the decoder circuit on separate nodes thereof" as recited in claim 13 and similarly recited in claim 24; "writing into a first register in a bus interface; latching a second STC timestamp into a second register in the bus interface, wherein the writing into the first register causes the second STC timestamp to be latched into the second register; and retrieving the second STC timestamp to the decoder by the way of the second register" as recited in claim 20 and similarly recited in claim 24; and "adjusting a STC frequency based on the comparison result by using firmware within the receiver circuit" as recited in claims 4 and 20 and similarly recited in claims 13 and 24.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ngoc K. Vu whose telephone number is 571-272-7306. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John W. Miller can be reached on 571-272-7353. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ngoc K. Vu Primary Examiner Art Unit 2611

March 13, 2006